DOC Code: AP.PRE.REQ

PTO/SB/33 (08-08)
Approved for use through 09/30/2008. OMB 0651-0031
United States Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
059864.01778

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Name _____

Application Number:

10/518,930

Filed: January 13, 2005

First Named Inventor:

Tommi KOISTINEN

Art Unit: 2446

Examiner: Shaq Taha

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96)

☒ Attorney or agent of record.
Registration No. 54,749

☐ Attorney or agent acting under 37 CFR 1.34.
Registration Number if acting under 37 CFR 1.34 _____

Signature

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703-720-7898
Telephone number

July 9, 2009
Date

NOTE: Signatures of all of the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	Confirmation No.: 7618
Tommi KOISTINEN et al.	Art Unit: 2446
Application No.: 10/518,930	Examiner: Shaq Taha
Filed: January 13, 2005	Attorney Dkt. No.: 059864.01778

For: LOAD BALANCING DEVICES AND METHOD THEREOF

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 9, 2009

Sir:

In accordance with the Pre-Appeal Brief Conference Pilot Program guidelines set forth in the July 12, 2005 Official Gazette Notice, Applicants hereby submit this Pre-Appeal Brief Request for Review of the final rejections of claims 26-37 and 41-57 in the above identified application. Claims 26-37 and 41-57 were finally rejected in the Office Action dated May 4, 2009. Applicants hereby appeal these rejections and submit this Pre-Appeal Brief Request for Review.

The final Office Action rejected claims 26-37, 41-47, and 49-56 under 35 U.S.C. §103(a) as being unpatentable over Kaniyar (U.S. Patent Pub. No. 2003/0187914) in view of Aviani (U.S. Patent No. 6,976,085). Applicants submit that there is clear error with regard to the obviousness of at least one element of claims 26-37, 41-47, and 49-56, as will be discussed below.

Applicants respectfully submit that Kaniyar and Aviani, whether considered alone or in combination, fail to disclose or suggest all of the elements of the present claims and that the final rejection is therefore clearly in error. For example, the combination of Kaniyar and Aviani does not disclose or suggest, at least, "selecting on a per received packet basis, by a load balancer configured to distribute load to said processors, a processor having a lowest load in such a manner that a respective next received packet is distributed to the processor irrespective of a

specific connection to which this next received packet belongs," as recited in claim 26, and the similar limitations recited in claims 41 and 50-54. Thus, according to embodiments of the invention, a received data packet is distributed to one of the processors irrespective of a specific connection to which the received packet belongs.

Kaniyar and Aviani fail to disclose or suggest that a processor having a lowest load is selected, on a per received packet basis, in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs. The Office Action erroneously took the position that paragraph 0031 of Kaniyar discloses this limitation of the claims (see Office Action, page 3). Paragraph 0031 of Kaniyar discloses that the least busy processor in the system can be selected as a "scheduling processor." Therefore, this section of Kaniyar is directed to choosing a "scheduling processor," which is the processor that determines which processor in the system will process the packet. Accordingly, in Kaniyar, one of the processors is selected as the load balancing processor or "scheduling processor."

According to embodiments of the invention, on the other hand, the load balancing unit selects a processor to process a received packet based on a lowest load and irrespective of a specific connection to which the received packet belongs. Kaniyar, however, fails to disclose selecting a processor to process the received packet irrespective of a specific connection to which the received packet belongs. In fact, Kaniyar appears to teach the opposite. Particularly, Kaniyar discloses that its system "ensures data packets received from the same network connection are routinely scheduled for processing by the same selected processor" (Kaniyar, paragraph 0008). Similarly, paragraph 0033 of Kaniyar states that "data packets associated with the same network connection are destined to be processed on the same selected processor... This method of systematically partitioning data streams for connections across processors enables a connection state to live on a single processor for the lifetime of the connection which, in turn, enhances performance of the multiprocessor system" (Kaniyar, paragraph 0033).

Therefore, according to Kaniyar, the "scheduling processor" selects the processor that has previously processed packets from the same network connection. In other words, Kaniyar teaches that packets received from the same network connection are scheduled for processing by the same processor, so that each connection state lives on a single processor for its lifetime

(Kaniyar, paragraphs 0007, 0008, 0033). Thus, the goal of Kaniyar is to systematically partition data streams in a manner that enable a connection state to live on a single processor for the lifetime of the connection (Kaniyar, paragraph 0033). As a result, the system disclosed in Kaniyar directly contradicts the claimed distribution of a received data packet to one of the processors irrespective of a specific connection to which the received packet belongs.

Furthermore, as discussed above, Kaniyar describes a method that enables a connection state to live on a single processor for the lifetime of the connection as being particularly beneficial (Kaniyar, paragraph 0033). Thus, a person of ordinary skill in the art would not be motivated to modify Kaniyar to relinquish the concept of assigning connections to processors statically since this concept is identified as being particularly advantageous.

However, the weakness of Kaniyar, which is overcome by the present application, is that for connections that are bursty, and due to random variation in activity, connections allocated to a first processor are in active phases causing the first processor to be highly loaded. While connections allocated to a second processor are idle, causing the second processor to be lightly loaded. Then, an incoming packet on a connection allocated to the first processor will be, according to Kaniyar, routed for processing by the highly loaded first processor, while the second processor is idle. Embodiments of the present invention overcome these drawbacks because, according to the present application, the lightly loaded processor would be selected to process the incoming packet since load balancing is done on a packet-by-packet basis irrespective of a specific connection to which the packet belongs.

In view of the above, Applicants respectfully submit that Kaniyar fails to disclose or suggest "selecting on a per received packet basis... a processor having a lowest load in such a manner that a respective next received packet is distributed to the processor **irrespective of a specific connection to which this next received packet belongs**," (emphasis added) as recited in claim 26, and similarly recited in claims 41 and 50-54. Rather, in direct opposition to what is recited in the present claims, Kaniyar discloses that packets received from the same network connection are always scheduled for processing by the same processor, so that each connection state lives on a single processor for its lifetime.

Furthermore, Aviani does not cure these deficiencies in Kaniyar. Aviani, as discussed above, merely discloses inserting connection information into data packets. Aviani, like

Kaniyar, fails to disclose or suggest that a processor having a lowest load is selected, on a per received packet basis, in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs. Therefore, Applicants respectfully assert that the combination of Kaniyar and Aviani does not disclose or suggest "selecting on a per received packet basis, by a load balancer configured to distribute load to said processors, a processor having a lowest load in such a manner that a respective next received packet is distributed to the processor irrespective of a specific connection to which this next received packet belongs," as recited in claim 26, and the similar limitations recited in claims 41 and 50-54. It is respectfully requested that the rejection of claims 26, 41, and 50-54 are in error and should be withdrawn.

Claims 27-37, 42-49, 55, and 56 are dependent upon claims 26, 41, and 54, respectively. As such, claims 27-37, 42-49, 55, and 56 should be allowed for at least their dependence upon claims 26, 41, and 54, and for the specific limitations recited therein.

Claim 48 was rejected under 35 U.S.C. §103(a) as being unpatentable over Kaniyar (U.S. Patent Pub. No. 2003/0187914) in view of Aviani (U.S. Patent No. 6,976,085), and further in view of Reimer (U.S. Patent Pub. No. 2002/0059502). Applicants submit this rejection is clearly erroneous for at least the following reasons.

Claim 48 is dependent upon claim 41 and inherits all of the limitations thereof. As discussed above, the combination of Kaniyar and Aviani fails to disclose or suggest all of the elements of claim 41. Furthermore, Reimer fails to cure the deficiencies in Kaniyar and Aviani, as Reimer also fails to disclose or suggest "selection circuitry configured to select, on a per received packet basis, one of a plurality of processors configured to perform communication in a packet switched connection on the basis of a stored load state of the selected processor in such a manner that a respective next received packet is distributed to the selected processor with a lowest load among said processors irrespective of a specific connection to which this next received packet belongs," as recited in claim 41. Thus, the combination of Kaniyar, Aviani and Reimer fails to disclose or suggest all of the elements of claim 48. In addition, claim 48 should be allowed for at least its dependence upon claim 41, and for the specific limitations recited therein.

Reconsideration and withdrawal of the rejections, in view of the clear errors in the Office Action, is respectfully requested. In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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Enclosures: PTO/SB/33 Form
Notice of Appeal
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